

Jetson Nano Developer Kit 40-Pin Expansion Header GPIO Usage Considerations

Application Note

Document History

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Introduction

This application note describes how to work with the signals on the 40-pin expansion header on the NVIDIA® Jetson Nano™ Developer Kit carrier board. All signals routed to this connector from the Jetson Nano module, except for the I2C interfaces, pass through TI TXB0108RGYR level shifters. This is necessary to level shift the signals from 1.8V levels from the module to 3.3V levels at the expansion connector pins. This level shifter retains the ability to pass bidirectional signals without the need for a direction pin. There are some considerations that must be considered when using the signals that come from (or go to) these level shifters. These considerations are described in this application note.

TXB0108 Level Shifter

Figure 1 shows the usage of the TXB devices and Figure 2 shows the TXB on the carrier board.

Figure 1. TXB Devices Typical Usage

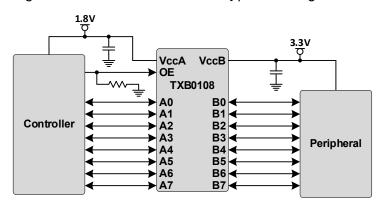
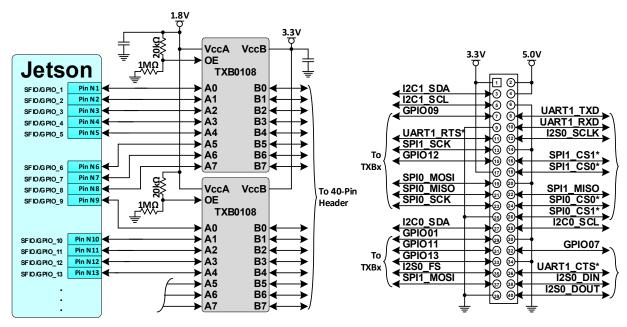


Figure 2. TXB Device Usage on Developer Kit Carrier Board



TXB Voltage Translator Architecture

The TXB push-pull buffered architecture supports bidirectional signaling without the need for a direction control signal to select whether a pin is an output or an input. This type of device is intended to interface with push-pull CMOS output drivers or high impedance loads, such as standard CMOS inputs. The TXB0108 devices are not intended for use in open-drain applications or to drive low impedance (i.e. directly driving an LED) or high capacitive loads (i.e. driving a long wire, or multiple loads). To support driving either of these load types, an additional buffer/transistor/FET may be required.

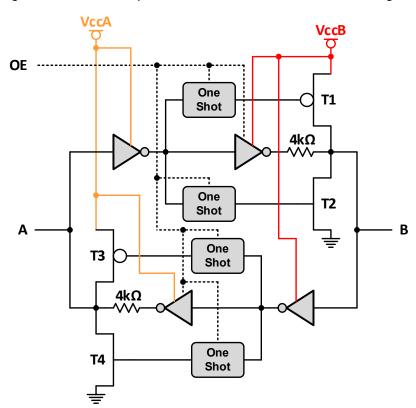


Figure 3. Simplified TXB0108 Architecture Diagram

The TXB level shifters have output buffers with $\sim 4k\Omega$ resistors in series which make them very weak. A one-shot (OS) circuit is included to help with signal rise/fall times. The OS circuitry is enabled when a rising or falling edge is sensed at one of the inputs.

When an A-port pin is connected to a push-pull driver output or a strong pull-up/down resistor (equivalent to a push-pull driver) and driven high, the weak buffer (w/series resistor) drives the B-port high along with the OS circuit which is enabled when the rising edge is sensed. The Bport is driven high by both the buffer and T1 until the OS circuit times out after which only the weak buffer continues to drive the output.

If, instead, the external push-pull driver drives the A-Port pin low, the B-port will be driven low along with the OS circuit which is enabled when the falling edge is sensed. The B-port is driven low by both the buffer and T2 until the OS circuit times out and only the weak buffer continues to drive the output. (See Figure 3).

The TXB-type level shifter is called "weak-buffered," because it is strong enough to hold the output port high or low during a DC state with a high impedance load, but weak enough that it can easily be over driven by a push/pull driver (or strong pull-up/down resistor). This allows the device to support inputs or outputs on both the A- and B-port sides.

An external push-pull driver or strong pull-up/down resistor must be able to supply more than ±2 mA of current to reliably overdrive the weak output buffer which is always active as long as the OE pin is active (high). If a pull-up/down resistor is used to force a TXB pin to a high/low state, similar to a push-pull driver, the resistor should be ~VccX/2 (~1.65kΩ or stonger if VccX is 3.3V, or $\sim 0.9 \text{k}\Omega$ or stronger if VccX is 1.8V.

"Keeper" Pull-up and Pull-down Resistors

If the design requires weak "keeper" pull-up and down resistors on any of the lines connected to the TXB devices, the resistors must be weak. When the TXB outputs are in a steady high and low state, the weak buffer with the $4k\Omega$ series resistor is driving the line. If an external "keeper" pull-up and down resistor is added, a resistor divider network is formed with the $4k\Omega$ series resistor. If the "keeper" resistor value is too small, the level driven by the TXB buffer may not meet a valid VOH (high) or VOL (low) level. This could lead to unreliable operation. The value of the external "keeper" resistor should be > $50k\Omega$. It is better not to have these "keeper" resistors whenever possible as they will have little effect when the TXB devices are powered. In the case of the Jetson Nano Developer Kit carrier board design, the TXB level shifters OE is active whenever the system is powered on. There are very weak $(1m\Omega)$ pull-downs on the OE pins to keep them disabled as the power comes on, and stronger (20k Ω) pull-ups to 1.8V to enable the TXB devices once power is enabled.

Driving Capacitive Loads

The TXB level shifters can drive up to about 70pF. If the load is much larger, the OS circuitry, which is enabled when a rising and falling edge is detected, is enabled for ~5ns. If the capacitive load is too large, the OS will timeout before the signal reaches a fully high or low level. After that, the signal will continue to rise and fall, but only driven by the weak output buffer which can lead to slower than desired rise and fall times.

Output Enable

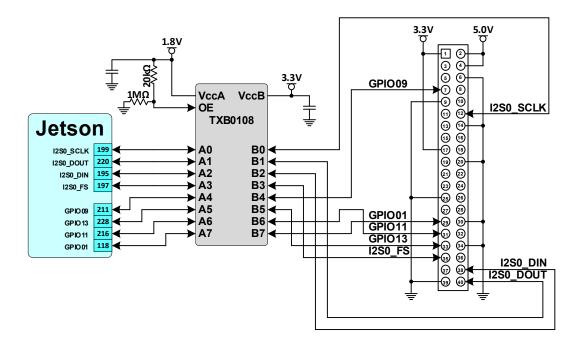
The TXB level shifters have an output enable (OE) pin. When low, the outputs (weak buffers and OS circuits) are disabled. When high, the weak buffers are enabled always, and the OS circuits are enabled when a rising and falling edge is detected. The Jetson Nano Developer Kit carrier board pulls the OE pins to 1.8V, so they are always enabled when the system is powered on.

Jetson Nano Developer Kit Examples

Following are several examples where pins from the 40-pin expansion header are connected to some device or circuit and some things to consider. The following figure shows eight signals from Jetson Nano that are routed to one of the TXB level shifters and then to the 40-pin expansion header. These signals support the following options on Jetson Nano:

- ▶ 12S0_SCLK: Audio 12S interface shift clock or GPIO
- ▶ 12S0 DOUT: Audio 12S interface shift clock or GPIO
- ▶ 12S0 DIN: Audio 12S interface shift clock or GPIO
- ▶ 12S0 FS: Audio 12S interface shift clock or GPIO
- ► GPI009: GPI0 or Audio Master Clock
- ► GPI013: GPI0 or PWM
- ► GPI011: GPI0 or General Purpose Clock
- ► GPI001: GPI0 or General Purpose Clock

Figure 4. One TXB Connection from Jetson Nano to 40-Pin Header



The following example shows possible connection of the Jetson Nano I2SO interface and GPI009 (Audio MCLK) Audio Codec.

GPIO09 Audio Codec I2S0_SCLK **►** SCLK **►** FS DIN **DOUT** MCLK GPIO01 GPIO11 GPIO13 ×12S0_FS 36) **③** 12SO DIN 37

I2S0_DOUT

⊛

<u>40</u>-**③**

Figure 5. Audio Codec (12S and MCLK) Example Connections

The following example shows possible connections to a button and an LED.

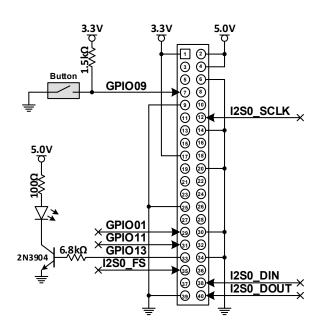


Figure 6. Button and LED Example Connections

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